UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/683,780	02/13/2002	James E. Bader	56162.00362	9493

21967 7590 06/14/2004

HUNTON & WILLIAMS LLP
INTELLECTUAL PROPERTY DEPARTMENT
1900 K STREET, N.W.
SUITE 1200
WASHINGTON, DC 20006-1109

EXAMINER	
SORRELL, ERON J	
ART UNIT	**PAPER NUMBER**
2182	5

DATE MAILED: 06/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/683,780	Applicant(s) BADER ET AL.	
	Examiner Eron J Sorrell	Art Unit 2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-44* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

FRITZ FLEMING
PRIMARY EXAMINER
GROUP 2100

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1,4-8,12,13,16-18,22,23,26-28,32,33,36-38,42, and 43 are rejected under 35 U.S.C. 102(b) as being anticipated by Marisetty et al. (U.S. Patent No. 5,792,598 hereinafter "Marisetty").

3. Referring to method claim 1 and 13, apparatus claim 23, and system claim 33, Marisetty discloses a method, apparatus and system, comprising:

connecting a first circuit component to the GPIO line (see item 104A connected to GPIO line 112)

connecting a second circuit component to the GPIO line concurrently with the first component (see item 104B connected to GPIO line 112)

wherein the first circuit component is to provide input to the integrated circuit using the GPIO line during a first time (see lines 48-54 of column 5); and

wherein the second circuit component is to receive an output from the integrated circuit using the GPIO line during a second time (see lines 48-54 of column 5).

4. Referring to method claims 4-8, method claim 16-18, apparatus claims 26-28, and system claims 36 and 37, Marisetty teaches the GPIO line services one I/O device at a time, and the desired I/O device has control of the bus during that time, until control is given to another I/O device at another time different from the previous time (see lines 25-54 of column 5).

5. Referring to method claim 12, method claim 22, apparatus claim 32, and system claim 38, Marisetty teaches the integrated circuit comprises a programmable logic array (see item labeled 103 in figure 1).

6. Referring to system claims 42 and 43, Marisetty teaches the system comprises a communications modem and the modem includes the first and second circuits (see lines 36-47 of column 5; Note the network controllers are interpreted as a modem).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 9-11,19-21,29-31, and 39-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Marisetty in view of AAPA (Applicant's Admitted Prior Art).

9. Referring to method claims 9-11, method claims 19-21, apparatus claims 29-31, and system claims 39-41, Mariesetty discloses the I/O devices can any I/O peripheral that can be coupled to the computer system (see lines 36-47 of column 5), however fails to explicitly set forth the limitation that the I/O devices are switches, light emitting diodes (LEDS), or an inverter.

The applicant admits on page 1, paragraph 2, that switches, light emitting diodes (LEDS), and inverters are typically

interfaced with GPIO lines and made use of by microcomputer systems.

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the method and system of Marisetty such that the I/O devices can be switches, LEDS, or an inverter in order to be used in a wide variety of applications.

10. Claims 2,3,14,15,24,25,34,35, and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Marisetty in view of Itay et al. (U.S. Patent No. 6,580,752 hereinafter "Itay").

11. Referring to method claims 2 and 3, method claims 14 and 15, apparatus claims 24 and 25, and system claims 34,35, and 44, Marisetty fails to teach the first component is further adapted to provide the first input at a low frequency relative to the switching frequency of the GPIO line and that the first time is concurrent with the second time.

Itay teaches a method and a system in a DSL environment wherein a first component is adapted to provide the first input at a low frequency relative to the switching frequency of the GPIO line and that the first time is concurrent with the second

time (see lines 3-16 of column 10; Note the claimed limitation is interpreted as multiplexed communication).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the method and system of Marisetty with the teachings of Itay such that the first component is further adapted to provide the first input at a low frequency relative to the switching frequency of the GPIO line and that the first time is concurrent with the second time in order for multi-channel communications can occur along the same lines simultaneously as suggested by Itay.

Response to Arguments

12. Applicant's arguments filed 3/30/04 have been fully considered but they are not persuasive. Applicant argues:

1) Marisetty fails to disclose each limitation of the independent claims as Marisetty does not disclose a GPIO line. Instead, Marisetty discloses a bus comprising several I/O lines (see paragraph bridging pages 11 and 12 and the first full paragraph of page 12 in applicant's remarks filed 3/30/04).

As per argument 1, the Examiner disagrees. Marisetty discloses the bus consists of several shared I/O lines (see lines 37-39 of column 5). Since Marisetty teaches at least one I/O line is

shared by more than one I/O device, Marisetty teaches the claimed limitation. There is no limitation in the claims that requires that only one of GPIO line be shared, or that there is only one GPIO line in the system.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eron J Sorrell whose telephone number is 703 305-7800. The examiner can normally be reached on Monday-Friday 9:00AM - 5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey A Gaffin can be reached on 703 308-3301. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

JEFFREY GAFFIN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EJS
June 9, 2004